REMARKS

Claims 10, 11, 12, 14, 15 and 18 have been amended, leaving claims 10-18 for consideration upon entry of the present Amendment.

The Office Action has been most carefully studied. No new matter has been entered by these amendments. As will be discussed in detail below, it is believed that the application is in condition for allowance.

The disclosure is objected to because of minor informalities. In particular, the Examiner objects to the use of the word "juncture" and states that the word "junction" should be used instead of "juncture." Applicants respectfully submit that the use of the word "juncture" is not a typographical error. The word "juncture" and "junction" mean the same thing. In Webster's Deluxe Unabridged Dictionary, Second Edition (1979) at page 992, "juncture" means a joining or being joined; the line or point at which two bodies are joined. "Junction" means the act of joining or the state of being joined; the place or point of union or meeting. The two words are synonymous and can be used interchangeably. Thus, Applicants have not modified the specification as suggested by the Examiner. Otherwise, Applicant has made the other changes requested to overcome the Examimer's objections. Applicant requests that the objections to the specification be withdrawn.

Claims 10 and 18 stand objected to because of minor informalities. Applicants herein amend Claims 10 and 18 to address the objections, thus the objection thereto may not be maintained. Further, Claim 12 is also amended to address minor informalities.

Claims 14-18 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that applicant regards as the as the invention. Claim 14 is amended to depend from Claim 11 to address insufficient antecedent basis for the terms as set forth therein. Claim 15 is amended to define the input impedance of the input stage circuit as being higher than a capacitance value of the parasitic capacitance. Accordingly, Applicants request that the rejection of claims 14-18 under 35 U.S.C. § 112, second paragraph be withdrawn.

Claims 10-18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Bowers (US 4,675,561). "A claim is anticipated only if each and every element as set forth in the claim is

found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 SPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, "[t]he identical invention must be shown in as complete detail as is contained in the * * * claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim 1, as amended, provides for the following limitation: "a parasitic capacitance is created between said pad and a semiconductor substrate, and said source of the source follower circuit is connected to the semiconductor substrate side of the parasitic capacitance **so as to charge and discharge the parasitic capacitance by the output signal of said source follower circuit**." (Emphasis supplied.) Support for the amendment to claim 1 is found on page 2, line 25 to page 3, line 5, page 4, line 8 to page 6, line 20, and Figure 1. Bowers does not disclose, teach, or suggest that limitation. Bowers teaches a CMOS output drive circuit having two field effect transistors (FETs) implemented with a CMOS process and parasitic bipolar transistors. Bowers does not teach or suggest a parasitic capacitance. Moreover, Bowers fails to teach or suggest that the source follower circuit directly drives a parasitic capacitance. Bowers also fails to teach or suggest that "said **source of the source follower circuit is *connected to* the semiconductor substrate side of the parasitic capacitance**." (Emphasis supplied.) Thus, Bowers does not anticipate claim 10. In addition, claims 11-18 include all the limitations of claim 10 and thus, Bowers does not anticipate claims 11-18. Thus, for the reasons stated above, Bowers does not anticipate claims 11-18. Applicants respectfully request withdrawal of the rejection as to claims 10-18.

Attached hereto is a marked-up version of the changes made to the specification and the claims. The attached page is captioned "**Version with Markings to Show Changes Made.**"

In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance issued. If the Examiner believes that a telephone conference with Applicants' attorneys would be advantageous to the disposition of this case, the Examiner is cordially requested to telephone the undersigned.

In the event the Commissioner of Patents and Trademarks deems additional fees to be due in connection with this application, Applicants' attorney hereby authorizes that such fee be charged to Deposit Account No. **06-1130.**

Respectfully submitted,

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Version with markings to show changes made.

IN THE SPECIFICATION:

A "marked-up" version of the Specification is as follows:

Please amend the specification at the first paragraph on page 4 beginning at line 7 in "marked up" format, as follows:

"The pad is connected to the buffer circuit 6. The buffer circuit 6 has its output terminal connected to the juncture between the parasitic capacitances 3 and 4. The parasitic capacitance 3, as shown in Fig. [4] 1, corresponds to a MOS capacitance created between the pad 1 and the island region 102. The parasitic capacitance 4 corresponds to a junction capacitance created between the island region 102 and the substrate. Thus, the output terminal of the buffer circuit 6 is connected to the island region 102."

Please amend the specification at the first paragraph on page 6 beginning at line 7 in "marked up" format, as follows:

"Moreover, since it is not required to boost the drive capability of the buffer circuit 6, the parasitic capacitance 4 can be charged and discharged by the source current of the J-FET. The so-called J-FET source follower circuit can [dis]charge and discharge the parasitic capacitance 4. This makes it possible to use a combination of the J-FET 2 and the buffer circuit shown in Fig. 1. Fig. 2 shows an embodiment where the J-FET 2 and the buffer circuit 6 are used as one unit. Referring to Fig. 2, the source of the J-FET 2[1] produces and output signal and the source follower circuit of the J-FET 2[1] charges and discharges the parasitic capacitance 4. That is, the source of the J-FET 2 is connected to the island region 102 and the parasitic capacitances 3 and 4 are charged and discharged by the output of the J-FET 2. Referring to Figs. 1 and 2, the J-FET 2 is used as the input stage circuit of the integrated circuit. In addition, the circuit shown in Figs. 1 and 2 is applicable to an input stage circuit with a high input impedance, for example, an amplifier with a high input impedance including a buffer circuit."

IN THE CLAIMS:

A marked-up version of the claims is as follows:

10. (Amended/Marked up) A semiconductor integrated circuit comprising:

a pad to which an input signal is externally input;

a source follower circuit including a transistor having a gate connected to said pad and a source for producing an output signal;

[whereby] wherein a parasitic capacitance is created between said pad and a semiconductor substrate, and said source of the source follower circuit is connected to the semiconductor substrate side of the parasitic capacitance so as to charge [discharges] and discharge[s] [a] the parasitic capacitance [created between said pad and a semiconductor substrate] by the output signal of said source follower circuit.

11. (Amended/Marked up) The semiconductor integrated circuit defined in Claim 10, further comprising an island region on the upper surface of said semiconductor substrate containing impurities of a second conductivity type, and a pad formed on said island region via an oxide film; and wherein said semiconductor substrate contains impurities of a first conductivity type; and wherein [said] an output terminal of said source follower circuit is connected to said island region.

12. (Amended/Marked up) The semiconductor integrated circuit defined in Claim 11, wherein said island region is surrounded with an isolation region containing impurities of [a] said first conductivity type.

14. (Amended/Marked up) The semiconductor integrated circuit defined in Claim [10] 11, wherein said output terminal [of said buffer circuit] is connected to said island region by way of a metal conductor.

15. (Amended/Marked up) The semiconductor integrated circuit defined in Claim 10, wherein [the] an input impedance of [said] an input stage circuit is set to a first [high] value, and

the parasitic capacitance is set to as a second value, the first value being higher than the second value.

18. (Amended/Marked up) The semiconductor integrated circuit defined in Claim 17, wherein said field effect transistor has a drain connected to a power source, and a source connected to [the] a ground via a constant current source, for producing [an] said output signal.